

CLAIMS

What is claimed is:

1. A circuit for generating a reference current,
comprising:

5 a positive feedback loop coupled with a floating current
mirror; and

a negative feedback loop diverting current from the
floating mirror.

10 2. The circuit of claim 1, where the negative feedback
loop diverts current directly from the floating mirror.

3. The circuit of claim 1, where the negative feedback
loop diverts current from the floating mirror by using a voltage
15 follower.

4. The circuit of claim 1, wherein the circuit operates
with a minimum supply voltage of approximately the sum of a
transistor threshold voltage plus three drain saturation
20 voltages.

5. The circuit of claim 1, wherein the current mirror
includes a pair of p-channel transistors.

6. A method for providing a current reference,
comprising:

providing a current mirror circuit portion;
providing a positive feedback loop portion coupled with
5 the current mirror; and
providing a negative feedback loop portion diverting
current from the floating mirror.

7. The method of claim 6, wherein the operation of
10 providing the current mirror circuit portion includes providing
a pair of p-channel transistors.

8. The method of claim 6, wherein operation of providing
the negative feedback loop portion includes diverting current
15 directly from the floating mirror.

9. The method of claim 6, wherein the operation of
providing the negative feedback loop portion includes providing
a control of a common voltage of the current mirror.

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10. A circuit providing a current reference, comprising:
a current mirror including a first transistor and a second
transistor;
at least one resistor defining a voltage node;
25 a pull-down transistor; and
an output transistor;

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto;

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor;

5 and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor.

10 11. The circuit of claim 10, wherein the pull-down transistor has one end coupled with the current mirror and a gate coupled with the voltage node, so as the amount of current provided by the first transistor increases, the pull-down transistor diverts an amount of current received by the first
15 transistor.

12. The circuit of claim 10, wherein the first and second transistors are p-channel MOSFETS.

20 13. The circuit of claim 10, wherein the amount of current mirrored to the second transistor provides a bias signal to the output transistor.

14. The circuit of claim 10, wherein the circuit operates
25 with a minimum supply voltage of approximately the sum of a

transistor threshold voltage plus three drain saturation voltages.

15. The circuit of claim 10, wherein the pull-down
5 transistor is an n-channel MOSFET.

16. The circuit of claim 10, wherein the output transistor is an n-channel MOSFET.

10 17. The circuit of claim 10, further comprising:
a protection transistor coupled between the pull-down transistor and the current mirror.

18. The circuit of claim 17, wherein the protection
15 transistor is a p-channel MOSFET.

19. The circuit of claim 10, wherein a load is coupled to the output transistor, the load receiving the current reference.